

EXPRESS MAIL CERTIFICATE

DOCKET NO. : 201951/141

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Michael Joyner

TITLE : A VIDEO BUS FOR HIGH SPEED MULTI-RESOLUTION
IMAGERS AND METHOD THEREOF

Certificate is attached to the **Informal Drawings (11 pages)** of the
above-named application.

“EXPRESS MAIL” NUMBER: **EL640135719US**

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FIG. 1 is a schematic diagram of a prior art pixel circuit. The circuit includes a reset transistor (56) and a source follower transistor (58). The reset transistor (56) has its gate connected to a RESET signal and its source connected to a node (54). The source follower transistor (58) has its gate connected to a PG signal and its source connected to node (54). Node (54) is also connected to a resistor (18) leading to ground. The drain of the source follower transistor (58) is connected to a CDS (Correlated Double Sampling) block (55). The CDS block (55) is also connected to a Row Access signal. The circuit is powered by VDD and ground.

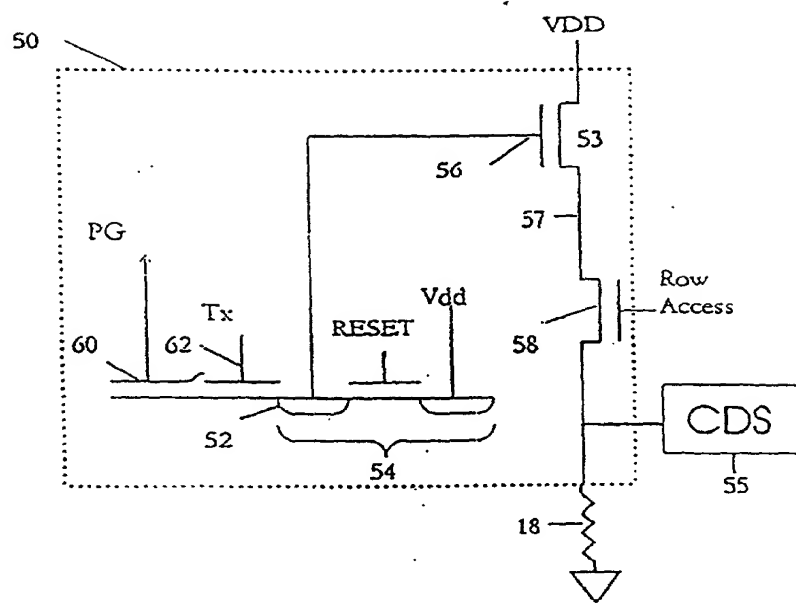


Figure 1
Prior Art

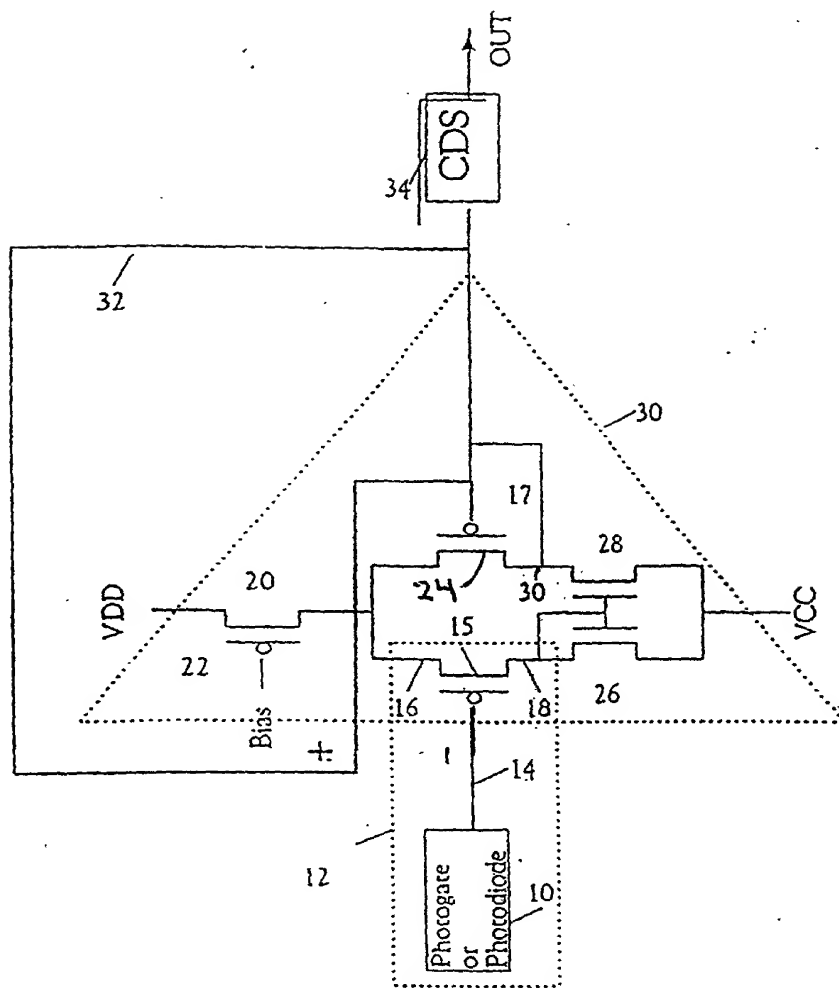


Figure 2

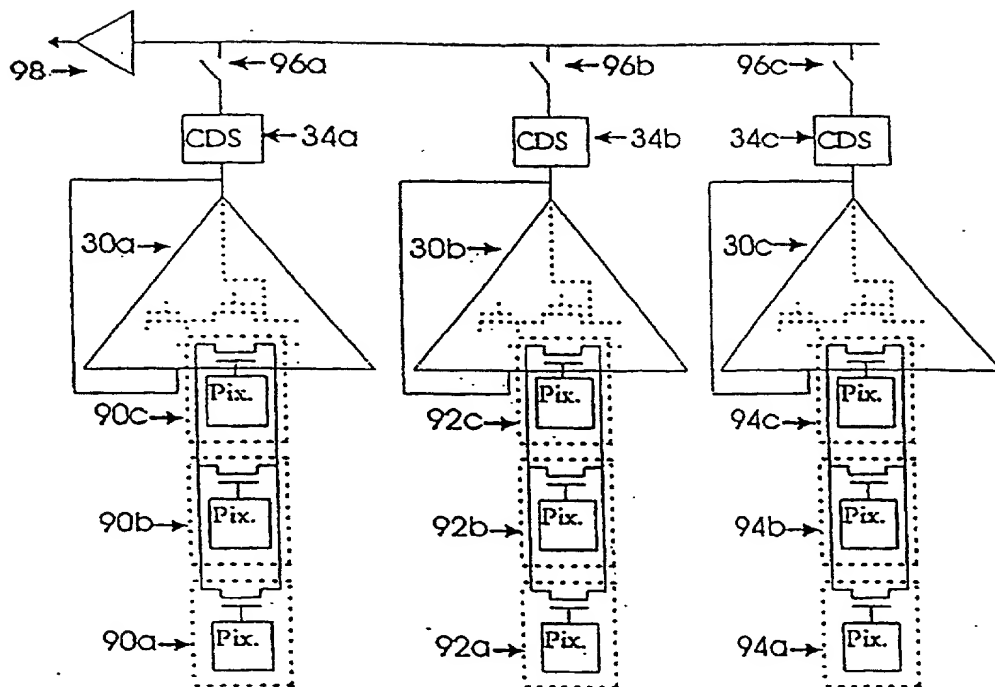


Figure 4

FIG. 6

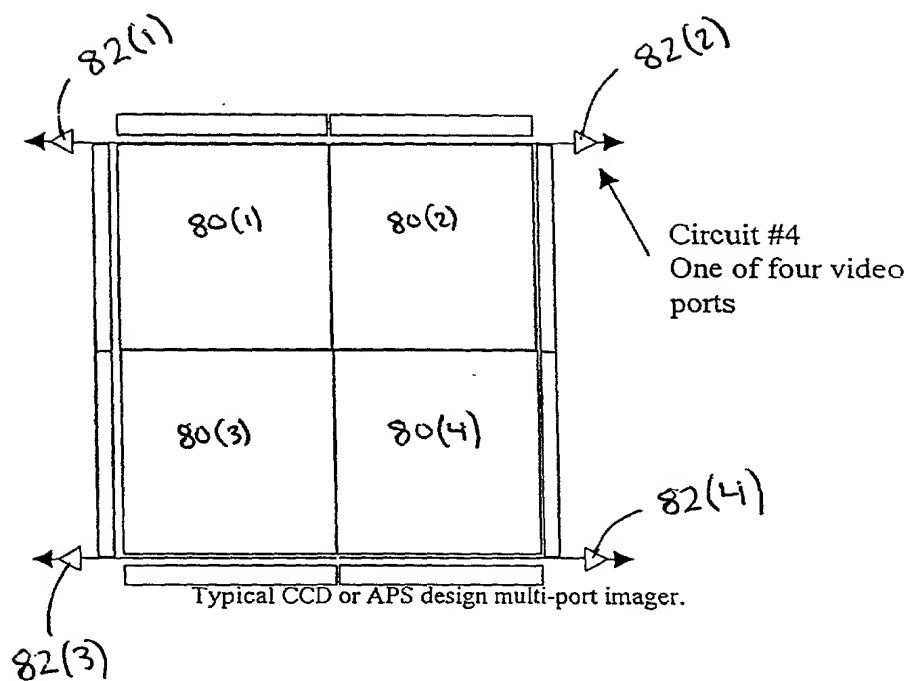
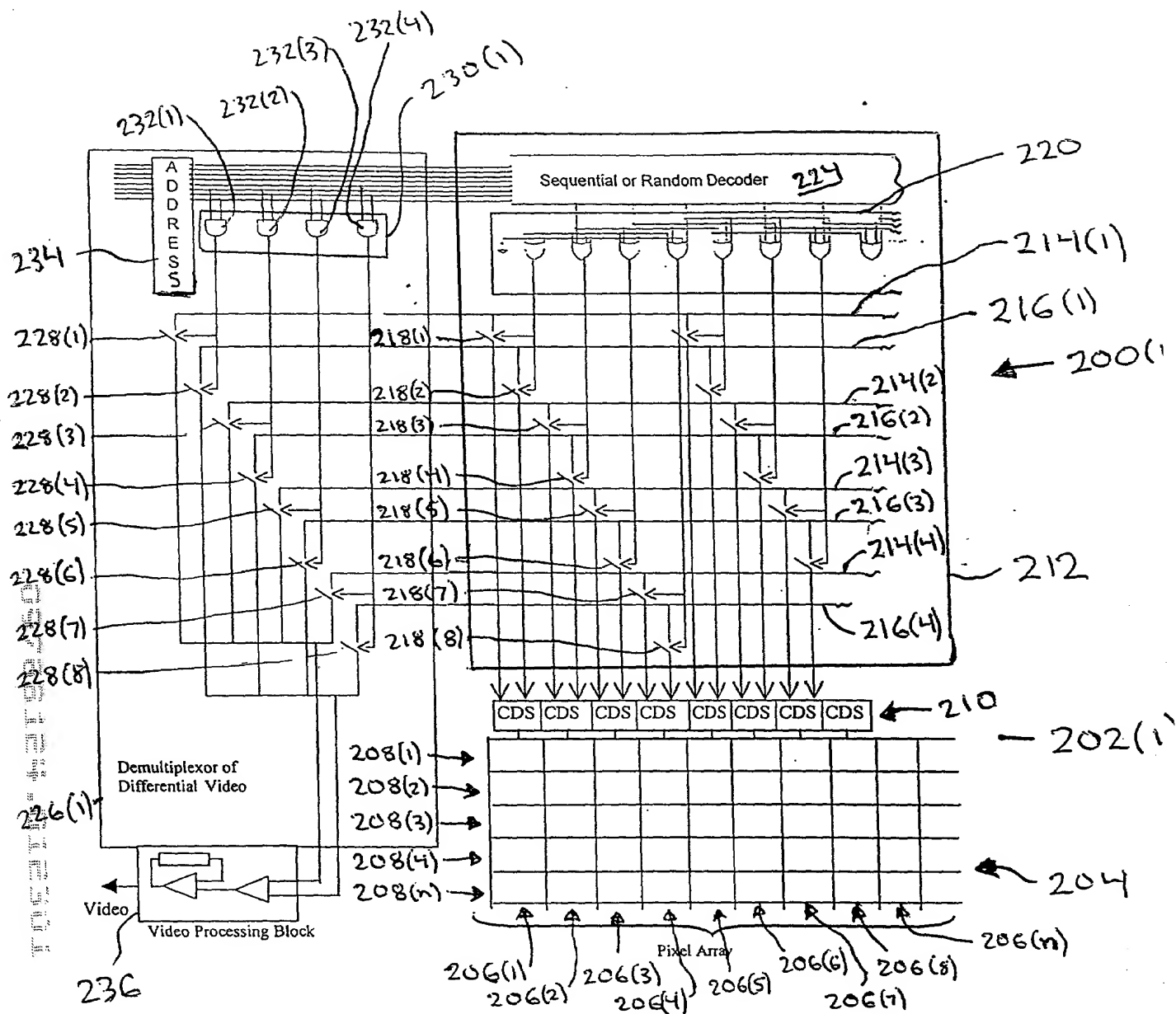


FIGURE 6



PVS Bus that eliminates multi-ports for high speed black and white

FIGURE 7A

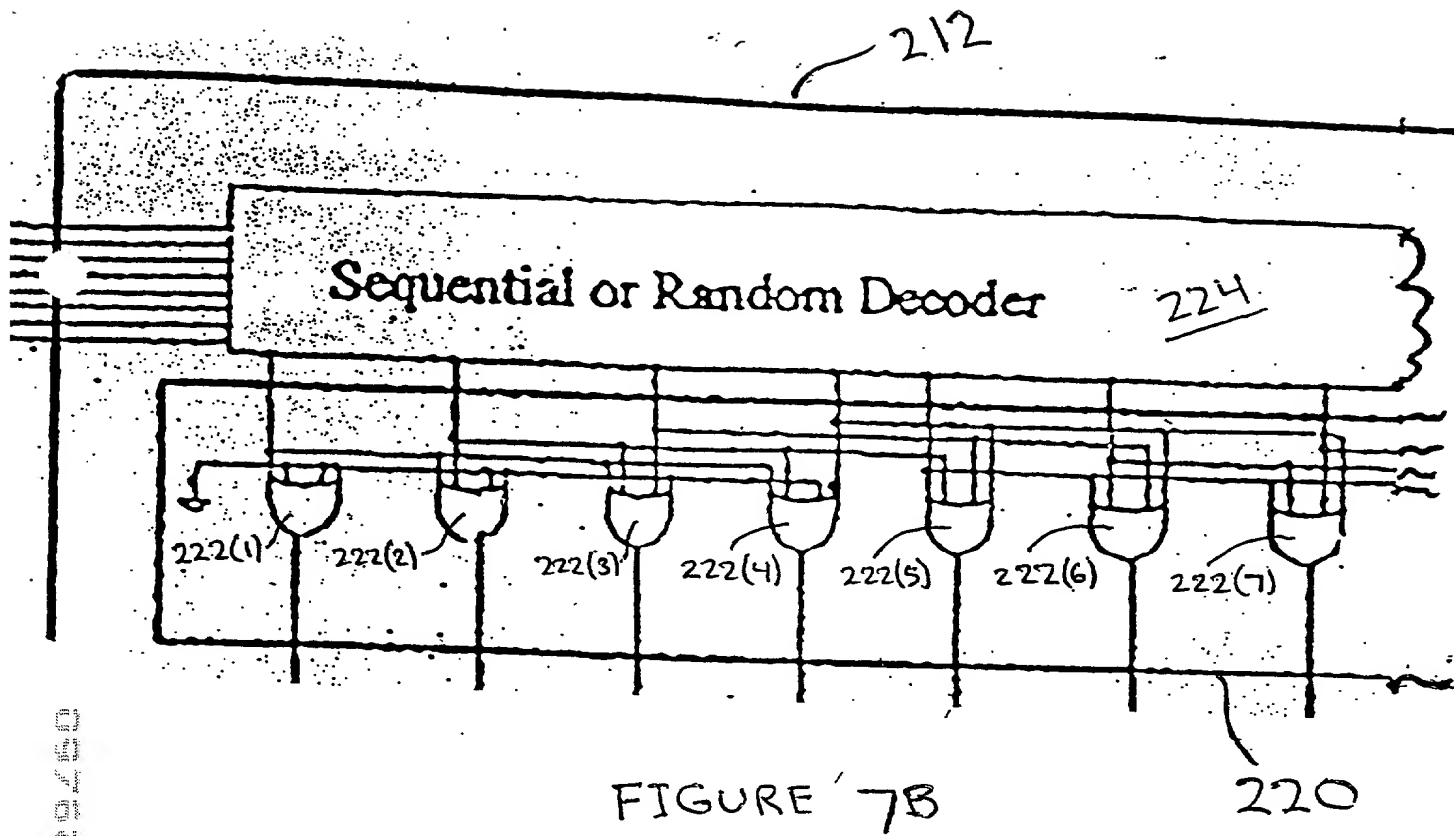


FIGURE 7B

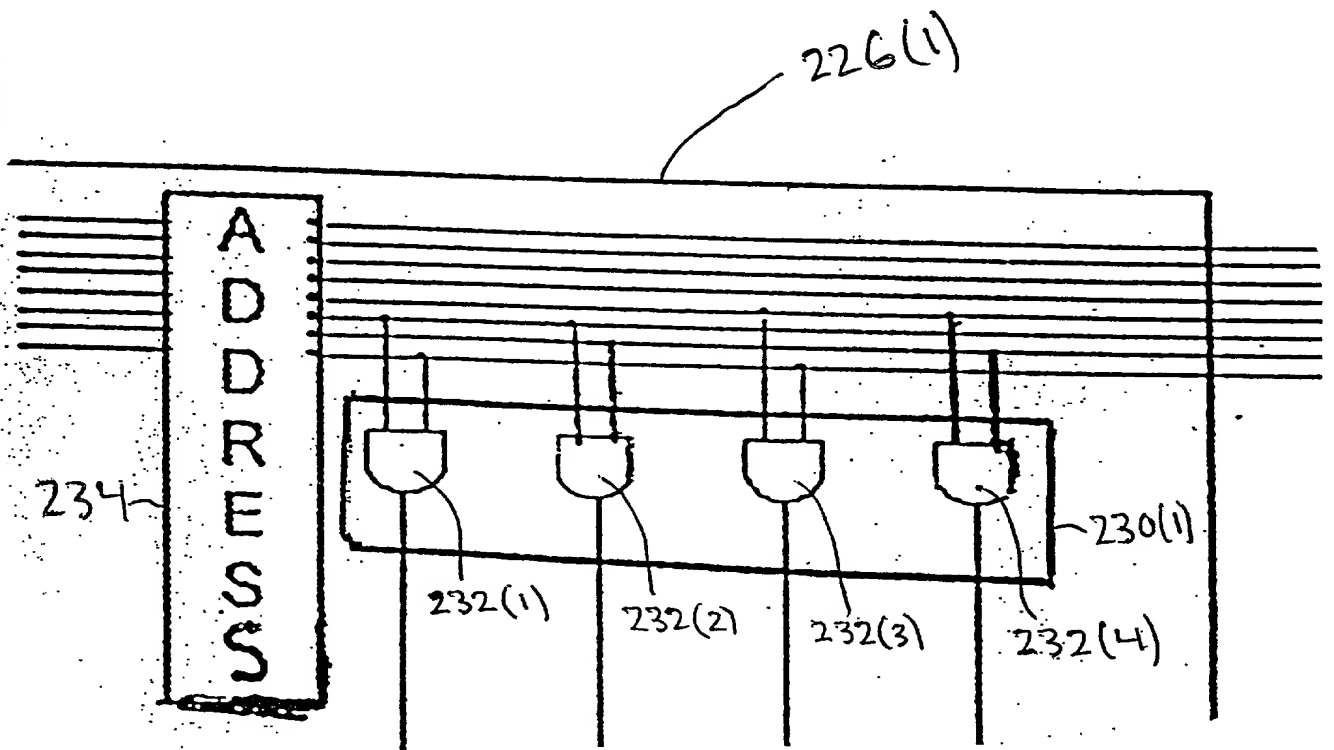


FIGURE 7C

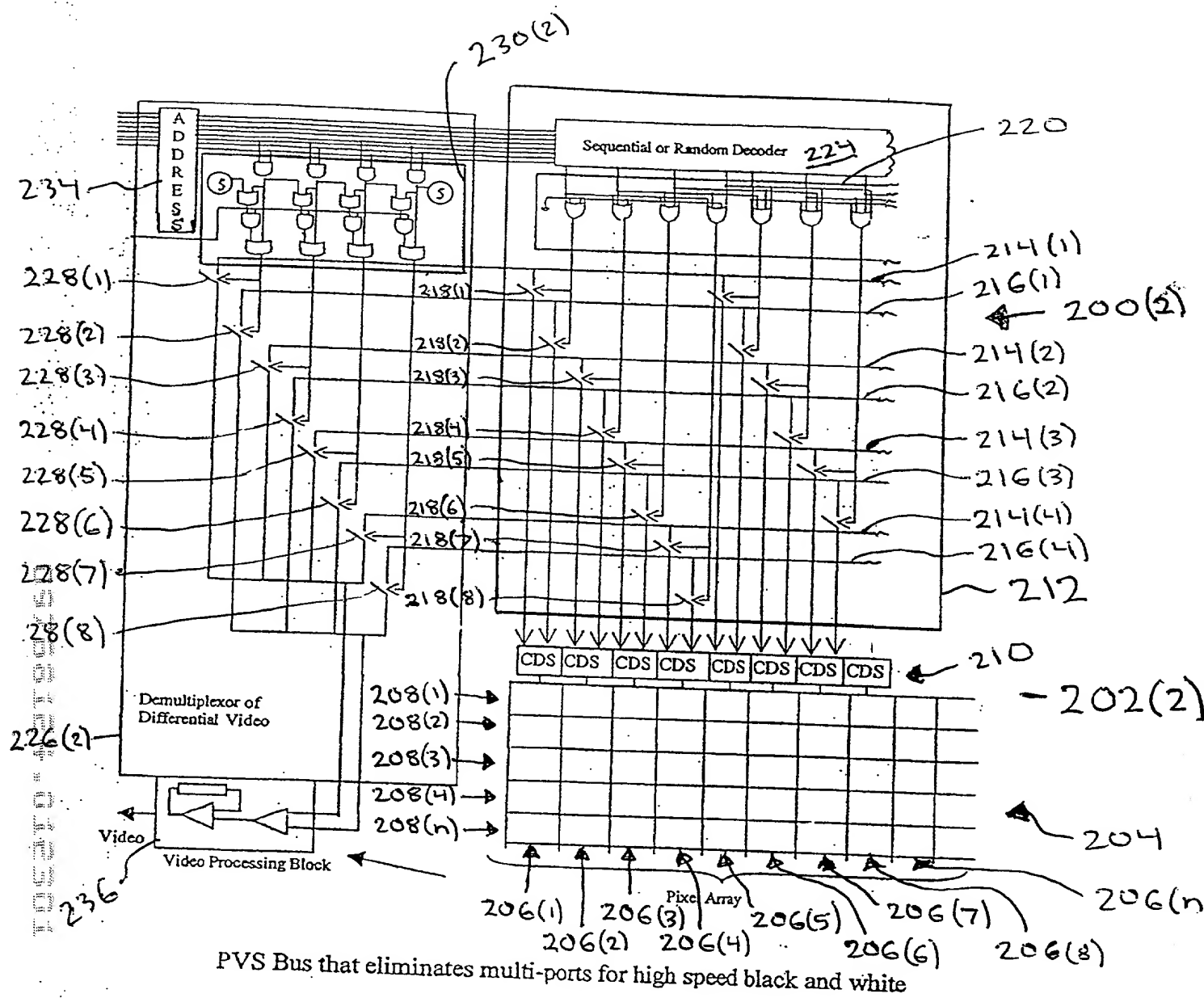


FIGURE 8A

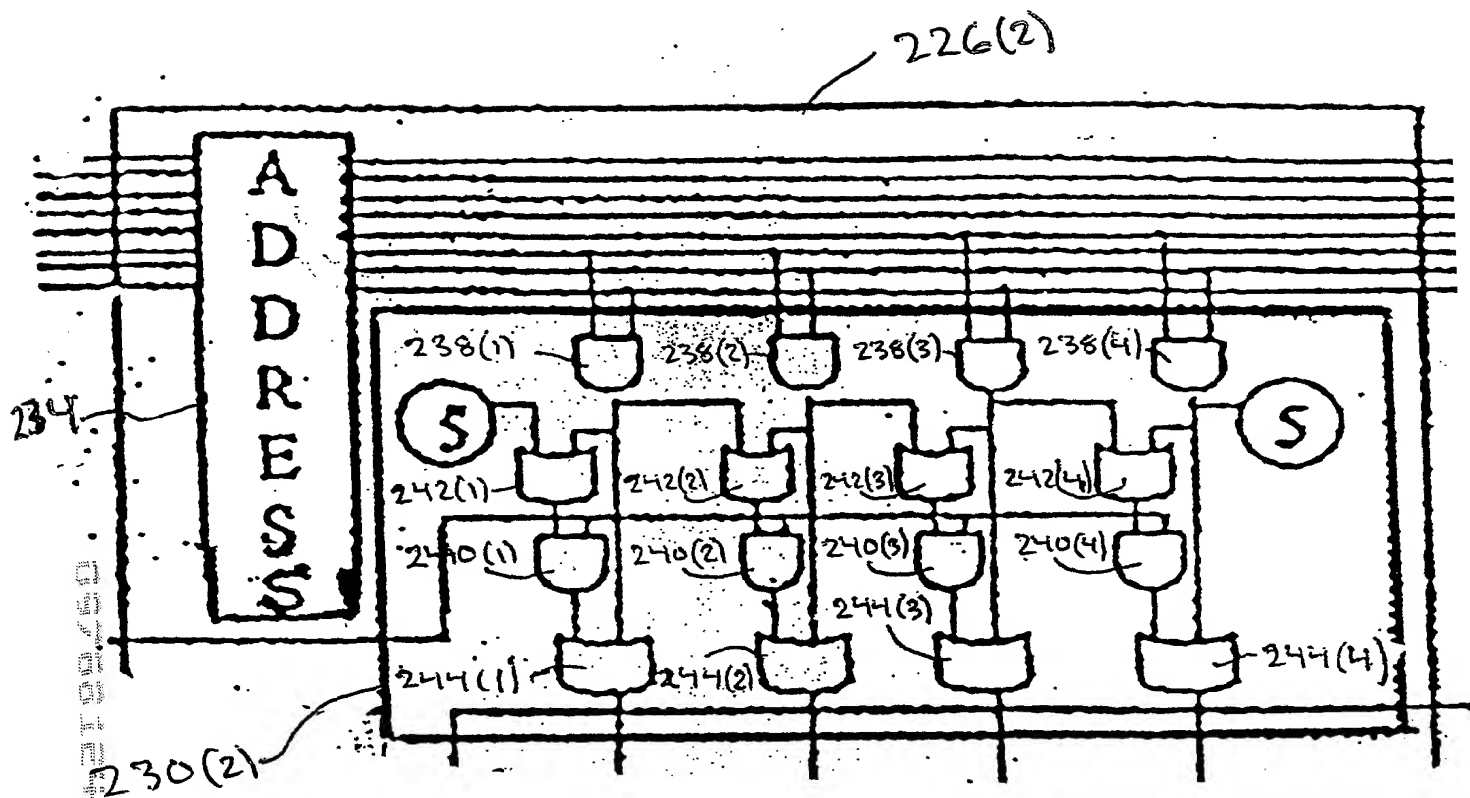


FIGURE 8B

FIGURE 9

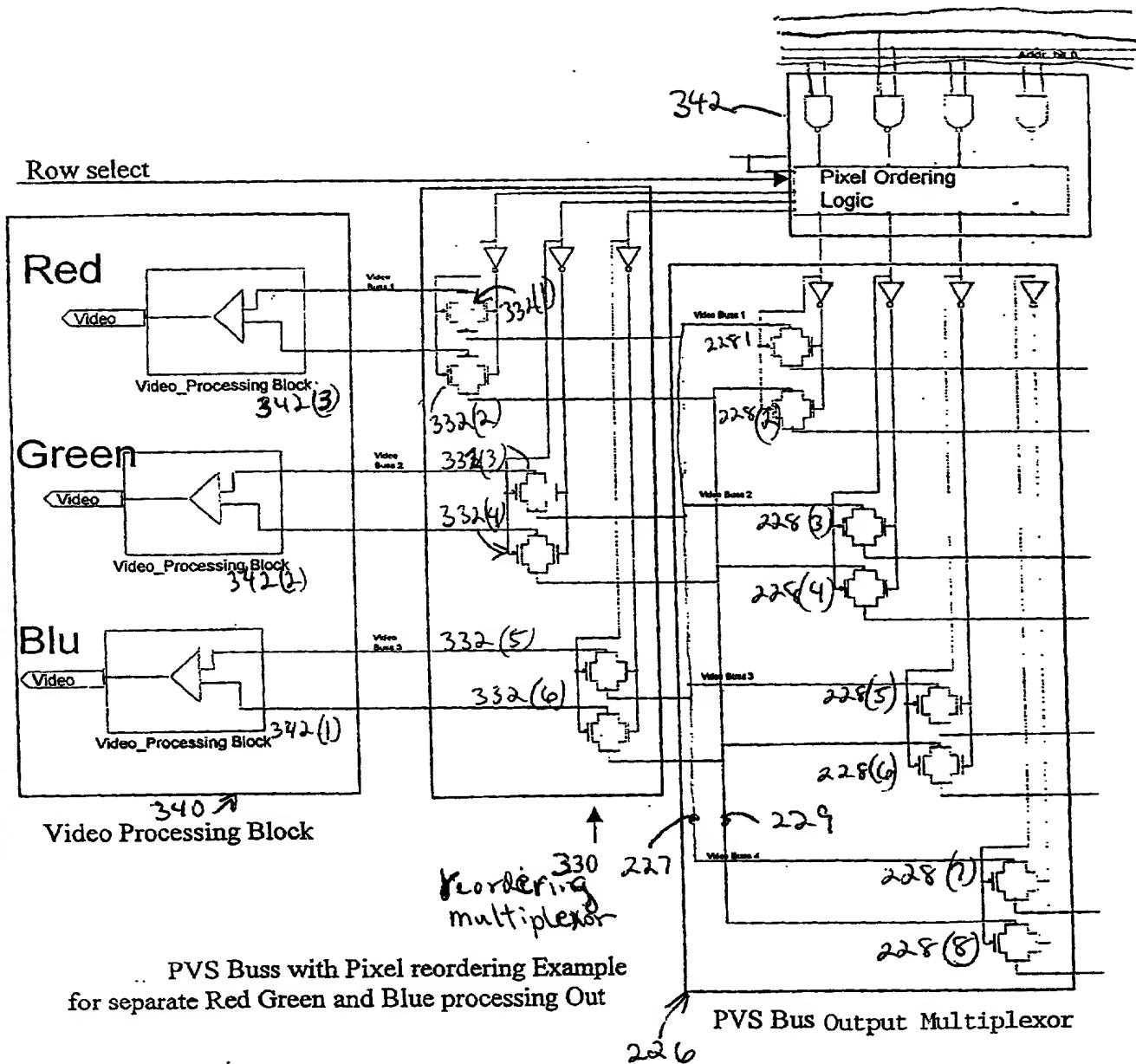


FIGURE 9